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High-Speed Hybrid-Logic Full Adder Low Power16-T XOR–XNOR Cell

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ABSTRACT

This paper presents 1-bit hybrid full adder cells circuit scheme that high speed and low power consumption. This Full adder cells circuit is designed utilization of XOR gate, XNOR gate, pass logic gate and transmission gate. Result of simulation by HSPICE program based on 90 nm CMOS technology with 1.2V power supply voltage and maximum frequency at 1GHz.

Keywords -CMOS technology, Full adder circuit, logic gate, High speed, Power.

INTRODUCTION

VLSI technology is basic of integrated circuit that used to component of transistor such as logic gate, full adder circuit and multiplication circuit. Design of integrated circuit is considered different of frequency, delay time, voltage, temperature, number of transistors, chip area and type of CMOS technology. This paper is designed high speed and low power of full adder circuit. At the present, telecommunication circuit are interested speed processor and low power consumption for demand. This paper presents 1 - bit hybrid full adder cells circuit to improve higher speed and lower power consumption. The proposed circuit uses 90 nm CMOS technology, voltage 1.2 V, maximum frequency 1 GHz and 1uF capacitance that compare with the other circuits 1-bit hybrid full adder cells circuit.

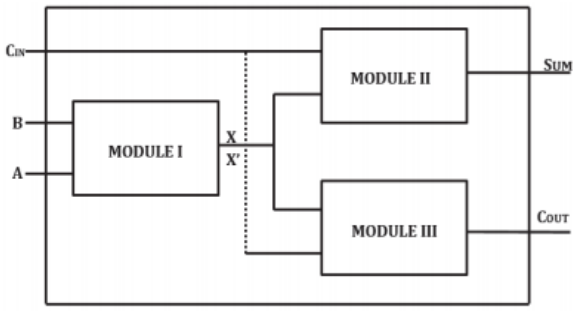

Fig. 1. Block diagram of hybrid logic FA circuit [6].

To realize a full adder (FA) circuit, several static CMOS logic styles have been presented [2] - [4]. These logic style scan be broadly classified into two categories: classical design style and hybrid design style. In classical design style, the FA is designed in a single module using MOS transistors. The complementary CMOS (C CMOS) FA [2] is an example of this approach. This design uses 28-transistors to realize pull-up and pull-down networks of a FA. It provides full swing outputs and robustness against voltage scaling and transistor sizing. The main drawback of this circuit is high input capacitance as each of the input is connected to the gates having at least a p MOS and an n MOS transistor which degrades the speed of the adder. Another example of the classical approach is complementary pass-transistor logic (CPL) FA [2]. This structure provides high speed, full swing output, and good driving capability because of the high-speed differential stage, cross-coupled PMOS structure, and static inverter at the output. However, the power dissipation of this circuit is high due to a large number of internal

nodes in the circuit. Also, the layout of this circuit is not symmetrical because of irregular transistor arrangement. In hybrid design style, FA structure is divided into three modules [3], [6], [7] as shown in Fig. 1. Module I generates full swing XOR and XNOR outputs of two input signals(A and B) simultaneously. These XOR–XNOR signals must have good driving capabilities as these signals have to drive other two modules. Module II and Module III are the sum and carry circuits which produce the sum and carry outputs(COUT), respectively, using the outputs of Module I and third input signal (CIN). The main advantage of hybrid style is that all the modules can be optimized at the individual level, and the number of transistors can be reduced, which reduces the internal power dissipating nodes. The performance of hybrid style FAs is as good as a single unit or small chains; however, they lack driving capability in higher bit adders implemented through cascading stages [8]. Various researchers have presented FA designs using hybrid logic style which provide optimum performance without degrading the output. Vastraback et al. [9] presented an XOR–XNOR module using pass transistors logic (PTL) in which sum and carry modules have been realized using2 to 1 multiplexer circuit. Zhang et al. [10] presented a hybrid FA cell in which PTL is used to generate XOR–XNOR outputs simultaneously, and C-CMOS style is used to implement carry module. In another design, New low-power and high-speed(LPHS) adder [11], XOR–XNOR circuit has been implemented using feedback transistor, while sum and carry modules are implemented using PTL and 2 to 1 multiplexer, respectively. Performance of XOR-XNOR circuit plays a vital role int he performance of hybrid FA design. Various approaches to designing XOR–XNOR circuit are presented in recent years. These approaches can be broadly classified into two categories. In the first approach, the XOR circuit is synthesized initially, and then XNOR output is generated using an inverter[e.g., transmission gate adder (TGA)]. This approach has a drawback that XOR and XNOR outputs are not generated simultaneously, which increases the chance of generating false switching and glitches in the outputs of the modules II and III [12]. In another approach, the XOR–XNOR circuit is designed such that XOR and XNOR outputs are generated simultaneously. In this approach, the delay difference between XOR and XNOR signals is tried to be minimized. An XOR–XNOR circuit using CPL is presented in [6] that gives the simultaneous generation of XOR–XNOR outputs. The output voltage levels in this circuit are recovered using the feedback transistors. However, the delay and power of this circuit remain higher due to feedback transistor. Goelet al. [3]eliminated the NOT gate from the critical path, however, the circuit delay remains higher due to the cross-coupled structure. Radhakrishnan [13] had presented a design of XOR–XNOR circuit with only six transistors. In this design, two complementary feedback transistors are used to restore the weak logic in complementary output nodes (XOR and XNOR) when both the inputs have same values (either “00” or “11”). This circuit suffers from the high worst case delay for the inputs“11” or “00” as in these cases; outputs reach their final voltage levels in two steps. This issue of slow response is resolved by Chang et al. [4] who used two additional nMOS and pMOS transistors at the XOR and XNOR output nodes, respectively. This circuit provides good driving capability and full output swing. However, the cross-coupled structure adds an extra parasitic capacitance to the XOR–XNOR output nodes. The structure of a XOR–XNOR circuit is further improved by Valashani and Mirzakuchaki [14] who used an inverter. This structure provides lower critical path delay, however, power dissipation remains higher. Naseri and Timarchi [15] presented an improved design of the XOR–XNOR circuit, which is implemented using 12 transistors. This circuit consumes low power and provides better delay performance than those of other circuits. However, this circuit requires an external inverter. The performance of this circuit can be improved further by eliminating this external inverter. In this article, a new XOR–XNOR circuit is proposed, which provides good driving capabilities and full

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swing XOR–XNOR outputs without using any external inverter. In this design, a feedback circuitry and internal NOT gate help in getting full swing output for all the transitions. By proper sizing of different transistors, not only the delay but also the power consumption of the proposed circuit is reduced. Using the proposed XOR–XNOR circuit, four different designs of FAs are also presented in this article. The proposed FAs show improvement in terms of power delay product (PDP)and driving capability than those of other structures.

II FULL ADDER CIRCUIT

Full adder circuit is digital circuit that used addition of binary numbers method. The output values of 1-bit full adder circuit are summary (SUM) and output carry (COUT) that according to binary number A, B and input carry (CIN) as shown on equation 1, equation 2 and table 1. Basic structure is shown in Fig. 2.

Sum=A+B+CIN (1)
COUT=(A.B)+(B.CIN)+(A.CIN) (2)

TABLE I.
TRUTH TABLE OF FULL ADDER CIRCUITS

INPUT			OUTPUT	
A	B	CIN	COUT	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

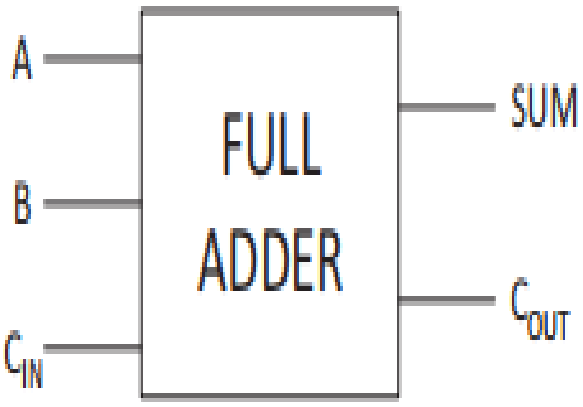

Fig 2. Basic structure of full adder circuit

III. PROPOSED CIRCUIT

The proposed circuit focus about high speed and low power consumption. The proposed circuit is designed by pass transistor logic and transmission gate. To decrease the complexity of design, the proposed Boolean equation are changed format as shown in equation 3 and 4. Therefore, the proposed circuit is shown in Fig. 3.

$$\text{Sum} = A \oplus B \oplus C_{IN}$$
$$= (A \oplus B) \cdot \overline{C}_{IN} + \overline{(A \oplus B)} \cdot C_{IN} \quad (3)$$

$$C_{OUT} = (A \cdot B) + (B \cdot C_{IN}) + (A \cdot C_{IN})$$
$$= (A \oplus B) \cdot C_{IN} + \overline{(A \oplus B)} \cdot A \quad (4)$$

The operation of proposed circuit is explained as follow:

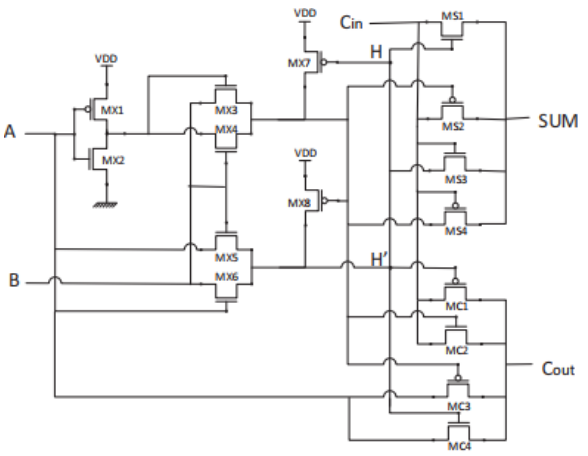

Fig. 3. Proposed circuit

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When input A is 0 and input B is 0, transistor MX1, MX3 and MX8 are turned on. So, output H is 0 and output H' is 1. After that input carry (CIN) is added. When input carry (CIN) is 0, transistor MS1, MS2, MS4 and MC3 are turned on. So, summary (SUM) value is 0 and output carry (COUT) value is 0. When input carry (CIN) is 1, transistor MS1, MS2, MS3, MC3 and MC4 are turned on. So, summary (SUM) is 1 and output carry (COUT) is 0.

When input A is 0 and input B is 1, transistor MX1, MX3, MX4, MX5 and MX7 are turned on. So, output H is 1 and output H' is 0. After that output carry (CIN) is added. When input carry (CIN) is 0, transistor MS4, MC1 and MC2 are turned on. So, summary (SUM) is 1 and output carry (COUT) is 0. When input carry (CIN) is 1, transistor MS3, MC1, MC2 and MC4 are turned on. So, summary (SUM) is 0 and output carry (COUT) is 1.

When input A is 1 and input B is 0, transistor MX2, MX6 and MX8 are turned on. So, output H is 1 and output H' is 0. After that input carry (CIN) is added. When input carry (CIN) is 0, transistor MS4, MC1 and MC2 are turned on. So, summary (SUM) is 1 and output carry (COUT) is 0. When input carry (CIN) is 1, transistor MS3, MC1, MC2 and MC4 are turned on. So, summary (SUM) is 0 and output carry (COUT) is 1.

When input A is 1 and input B is 1, transistor MX2, MX4, MX5, MX6 and MX8 are turned on. So, output H is 0 and output H' is 1. After that input carry (CIN) is added. When input carry (CIN) is 0, transistor MS1, MS2, MS4 and MC3 are turned on. So, summary (SUM) is 0 and output carry (COUT) is 0. When input carry (CIN) is 1, transistor MS1, MS2, MS3, MC3 and MC4 are turned on. So, summary (SUM) is 1 and output carry (COUT) is 1.

IV SIMULATION RESULTS

Simulation of circuit for performance in real situation, input and output buffer is added in the circuit as shown in Fig. 4.

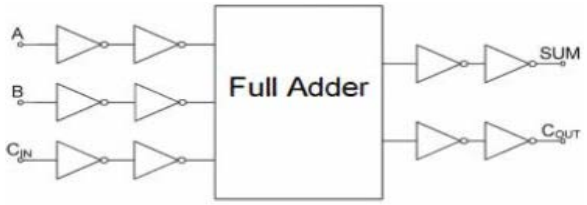

Fig. 4. Simulation of circuit

A HSPICE program is used to run simulations. The results are shown in Fig.5 and Fig.6 that simulation based on 90 nm CMOS technology, 1.2V with frequency 1GHz.

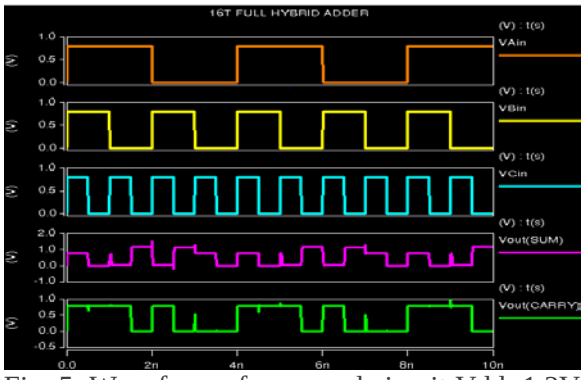

Fig. 5. Waveform of proposed circuit Vdd=1.2V, f =1GHz.

TABLE II
PERFORMANCE COMPARISON OF DIFFERENT FA CIRCUITS IN TERMS OF POWER DISSIPATION, PDP AT THE POWER SUPPLY OF 1.2 V AND OPERATING FREQUENCY OF 1 GHZ

Full adder circuits	Number of Transistors	Power (µW)
Zavaveri [18]	26	27
Valshani [17]	18	25
H.Naseri [15]	22	26.7
FA Design- 1	20	27.9
FA Design- 2	26	30.4
FA Design- 3	26	29.7
FA Design- 4	20	25.8
Proposed	16	23.3

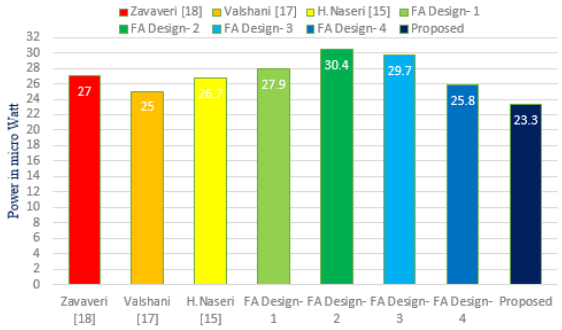

Fig. 6.Comparison different circuit power consumption.

A. Comparison of Power Consumption
The comparison of power consumption are compared 8 values that 1.2V by 90 nm CMOS technology, frequency is 1GHz and capacity load is 1fF with Zavaveri [18], Valshani [17],H. Naseri [15], FA Design- 1, FA Design- 2, FA Design- 3, FA Design- 4 and proposed circuit. The results are shown in Fig. 5-6 and Table2.

V CONCLUSION

The proposed 1-bit hybrid full adder cells circuit is designed by pass transistor logic and transmission gate with 16 transistors that high speed and low power consumption 23.3µW which is comparatively low with the different circuits. The simulation by HSPICE program with 90 nm CMOS technology, voltage 1.2V, frequency at 1GHz.This circuit can run maximum frequency at 1GHz.

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